This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-13 (cancelled)

1. ~~14.~~ (Currently Amended) A digital amplifier, comprising:

a summation circuit for summing an input signal with a feedback signal, and generating a summed output signal;

a noise shaping network with an input coupled to [~~the output of the~~] a summation circuit output and generating a noise shaped signal;

a sampling stage with an input connected to [~~the output of the~~] a noise shaping network output, and generating a sampled signal, the sampling stage having a predetermined sampling frequency, and generating [~~an~~] a sampling stage output signal with a lower transition rate with respect to the sampling frequency by a predetermined multiple;

a feedback loop providing the sampling stage output signal [~~of the sampling stage~~] coupled directly to the summation circuit; and

an output stage with inputs connected to [~~the output of the~~] a sampling stage output and generating an output signal.

2. ~~15.~~ (Previously Amended) The digital amplifier of claim ~~14~~ 1, wherein the output stage includes an H-bridge controller.

3. ~~16.~~ (Previously Amended) The digital amplifier of claim ~~14~~ 1, wherein the sampling stage further comprises a logic circuit for suppressing sampling of the input signal for a set number of clock cycles of the sampling frequency clock.

4. ~~17~~. (Previously Amended) The digital amplifier of claim ~~16~~ 3, wherein the logic circuit further includes a transition detector for detecting a transition in the output signal.

5. ~~18~~. (Currently Amended) The digital amplifier of claim ~~14~~ 1, wherein the sampling stage output signal [~~of the sampling stage~~] has a multi-state output, with at least three states.

6. ~~19~~. (Previously Amended) The digital amplifier of claim ~~14~~ 1, wherein the noise shaping network comprises a plurality of integrator stages.

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7. ~~20~~. (Currently Amended) A digital amplifier, comprising:

a summation circuit for summing an input signal with a feedback signal, and generating a summed output signal;

a noise shaping network with an input coupled to [~~the output of the~~] a summation circuit output and generating a noise shaped signal;

a sampling stage with an input connected to [~~the output of the~~] a noise shaping network output, and generating [~~an~~] a sampling stage output signal with a multi-state output, with an least three states;

a feedback loop providing the sampling stage output signal of the sampling stage coupled directly to the summation circuit; and

an output stage with inputs connected to [~~the output of the~~] a sampling stage output and generating an output signal.

8. ~~21~~. (Currently Amended) The digital amplifier of claim [~~14~~] ~~20~~ 7, wherein the output stage includes a semiconductor H-bridge controller.

9. ~~22~~. (Currently Amended) The digital amplifier of claim [~~14~~] ~~20~~ 7, wherein the sampling circuit generates [~~an~~] a sampling stage output signal with a lower transition rate with respect to the sampling frequency by a predetermined multiple.

10. ~~23~~. (Currently Amended) The digital amplifier of claim [~~14~~] ~~20~~ 7, wherein the sampling circuit further comprises a logic circuit for suppressing sampling of the input signal for a set number of clock cycles of the sampling frequency clock.

11. ~~24~~. (Currently Amended) The digital amplifier of claim [~~17~~] ~~23~~ 10, wherein the logic circuit further comprises a transition detector for detecting a transition in the output signal.

12. ~~25~~. (Currently Amended) The digital amplifier of claim [~~14~~] ~~20~~ 7, wherein the noise shaping network comprises a plurality of integrator stages.

Claims 26-27 (Cancelled)

13. ~~28~~. (Previously Added) A method of digital amplification, comprising:

summing an input signal with a feedback signal and generating a summed output signal;

noise shaping the summed output signal to generate a noise shaped signal;

sampling the noise shaped signal at a predetermined sampling frequency and generating a sampled output signal with a lower transition rate with respect to the predetermined sampling frequency by a predetermined multiple;

feeding back the sampled output signal as the feedback signal; and

outputting the sampled output signal as an output signal.

14. ~~29.~~ 13 (Previously Added) The method of digital amplification of claim ~~28~~, further comprising outputting the sampled output signal through an H-bridge controller.

15. ~~30.~~ 13 (Previously Added) The method of digital amplification of claim ~~28~~, wherein the sampling includes suppressing sampling of the noise shaped signal for a set number of clock cycles of a sampling frequency clock.

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16. ~~31.~~ 15 (Previously Added) The method of digital amplification of claim ~~30~~, wherein the suppressing sampling includes detecting a transition in the sampled output signal.

17. ~~32.~~ 13 (Previously Added) The method of digital amplification of claim ~~28~~, wherein the outputting includes outputting a multi-state output signal with at least three states.

18. ~~33.~~ 13 (Previously Added) The method of digital amplification of claim ~~28~~, wherein the noise shaping includes integrating the summed output signal through a plurality of integrator stages.

19. ~~34.~~ (Previously Added) A method of digital amplification, comprising:

summing an input signal with a feedback signal and generating a summed output signal;

noise shaping the summed output signal and generating a noise shaped signal;

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sampling the noised shaped signal and generating a sampled output signal;

feeding back the sampled output signal as the feedback signal; and

generating a multi-state output signal having at least three states using the sampled output signal.

20. ~~35~~ 19 (Previously Added) The method of digital amplification of claim ~~34~~, wherein a semiconductor H-bridge controller generates the multi-state output signal.

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21. ~~36~~ 20 (Previously Added) The method of digital amplification of claim ~~35~~, wherein the sampling includes generating a sampled output signal having a lower transition rate with respect to a sampling frequency by a predetermined multiple.

22. ~~37~~ 21 (Previously Added) The method of digital amplification of claim ~~36~~, wherein the sampling includes suppressing sampling of the noise shaped signal for a set number of clock cycles of a sampling frequency clock.

23. ~~38~~ 22 (Previously Added) The method of digital amplification of claim ~~37~~, wherein the suppressing sampling includes detecting a transition in the output signal.

24. ~~39~~ 23 (Previously Added) The method of digital amplification of claim ~~38~~, wherein the noise shaping includes integrating the summed output signal through a plurality of integrator stages.